PAGE 2/15 * RCVD AT 3/15/2005 9:03:14 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729306 * CSID:+972 3 7/103322 * DURATION (mm-ss):03-52

In the title:

Kindly amend the title as follows:

A method of creating a high performance virtual multiprocessor by adding a new dimension to a processor's pipeline. METHOD AND APPARATUS FOR CONVERTING A PROCESSOR INTO A COMPATIBLE VIRTUAL MULTITHREADED PROCESSOR (VMP)

In the Specfication:

At page 6, 3rd paragraph, bridging on to page 7, 1st paragraph, kindly amend as follows:

Reference is now made to Fig. 5, which is simplified flowchart illustration of a method of converting a computer processor into a multithreaded processor (VMP), operative accordance with a preferred embodiment of the present invention. In the method of Fig. 5 a single-threaded processor with a k-phased pipeline is converted into an n-threaded VMP with n*k-phased pipeline, where n is a whole number greater than one and k is a whole number greater than zero. The VMP is compatible with the original processor, being able to run the same binary code as the original processor modification. The VMP operates at a clock frequency that is up to n times higher than the original clock frequency, due to the n-fold deeper pipeline. Up to n interleaved threads. where each thread is independent program, are run simultaneously, The VMP compensates for pipeline penalties, such as stalling and idling, that are usually introduced when adding phases to a conventional pipeline.